

# PHK28NQ03LT

TrenchMOS™ logic level FET

Rev. 02 — 10 April 2003

Product data

## 1. Product profile

### 1.1 Description

N-channel enhancement mode field-effect transistor in a plastic package using TrenchMOS™ technology.

Product availability:

PHK28NQ03LT in SOT96-1 (SO8).

### 1.2 Features

- Logic level compatible
- Low gate charge.

### 1.3 Applications

- DC-to-DC converters
- Switched mode power supplies.

### 1.4 Quick reference data

- $V_{DS} \leq 30\text{ V}$
- $I_D \leq 23.7\text{ A}$
- $P_{tot} \leq 6.25\text{ W}$
- $R_{DS(on)} \leq 6.5\text{ m}\Omega$ .

## 2. Pinning information

Table 1: Pinning - SOT96-1 simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1,2,3	source (s)	<p style="text-align: center;">Top view MBK187</p>	<p style="text-align: center;">MBB076</p>
4	gate (g)		
5,6,7,8	drain (d)		



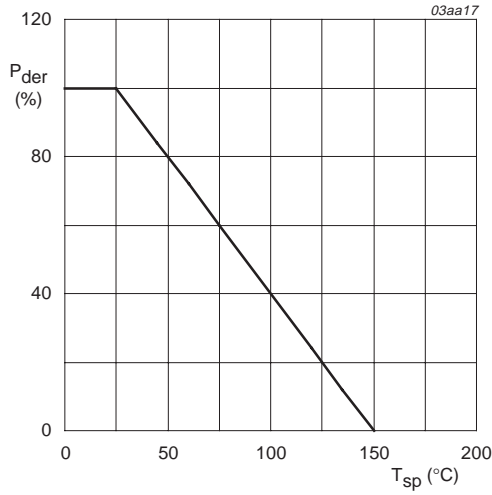
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### 3. Limiting values

**Table 2: Limiting values**

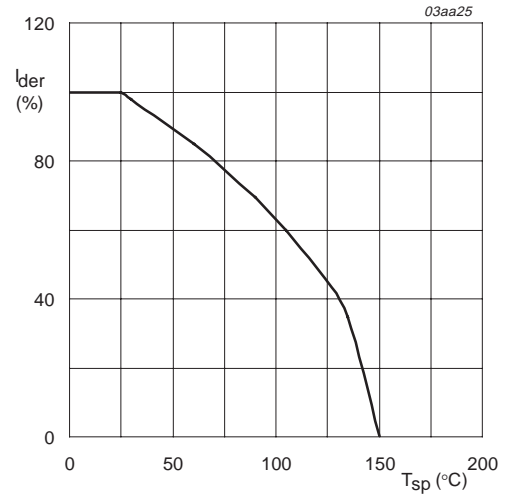
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	30	V
$V_{DGR}$	drain-gate voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$ ; $R_{GS} = 20\text{ k}\Omega$	-	30	V
$V_{GS}$	gate-source voltage		-	20	V
$I_D$	drain current (DC)	$T_{sp} = 25\text{ °C}$ ; $V_{GS} = 10\text{ V}$ ; <b>Figure 2 and 3</b>	-	23.7	A
		$T_{sp} = 100\text{ °C}$ ; $V_{GS} = 10\text{ V}$ ; <b>Figure 2</b>	-	15	A
$I_{DM}$	peak drain current	$T_{sp} = 25\text{ °C}$ ; pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; <b>Figure 3</b>	-	60	A
$P_{tot}$	total power dissipation	$T_{sp} = 25\text{ °C}$ ; <b>Figure 1</b>	-	6.25	W
$T_{stg}$	storage temperature		-55	+150	°C
$T_j$	junction temperature		-55	+150	°C
<b>Source-drain diode</b>					
$I_S$	source (diode forward) current (DC)	$T_{sp} = 25\text{ °C}$	-	5.2	A
$I_{SM}$	peak source (diode forward) current	$T_{sp} = 25\text{ °C}$ ; pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	20.8	A



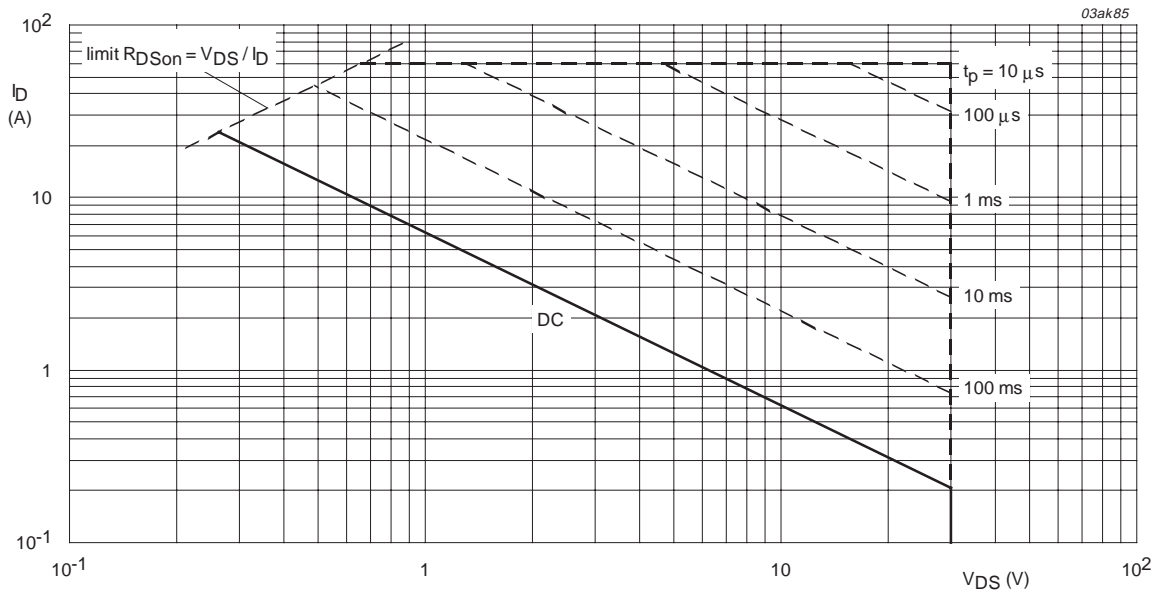
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of solder point temperature.



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of solder point temperature.



T<sub>sp</sub> = 25 °C; I<sub>DM</sub> is single pulse; V<sub>GS</sub> = 10 V

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

## 4. Thermal characteristics

Table 3: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	Figure 4	-	-	20	K/W

### 4.1 Transient thermal impedance

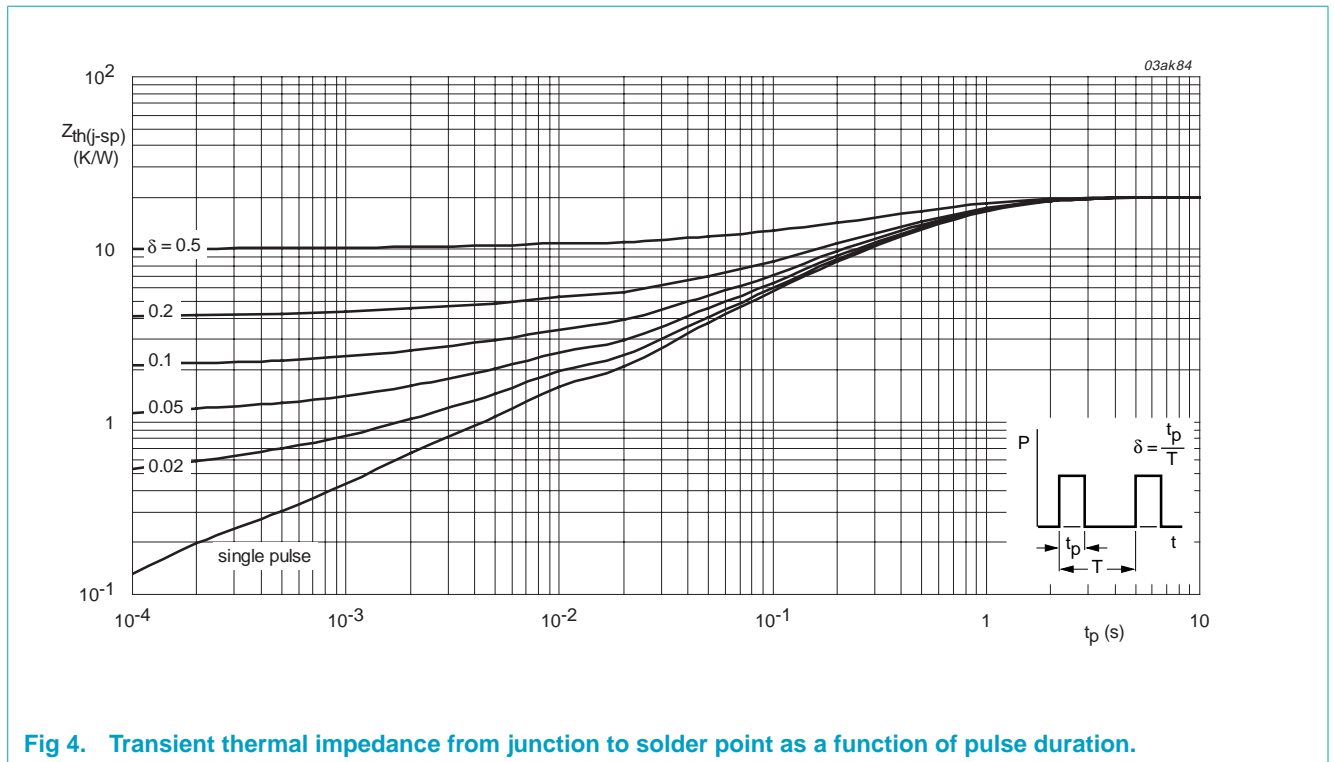
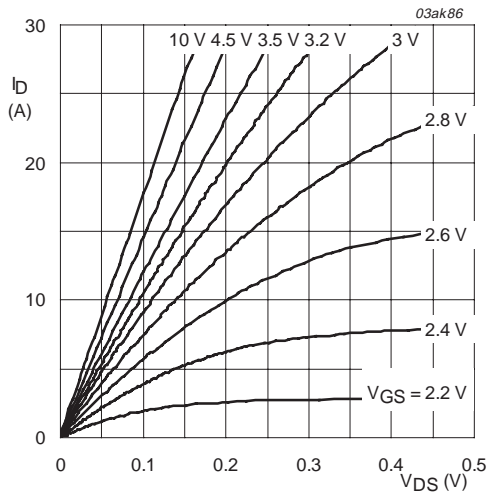


Fig 4. Transient thermal impedance from junction to solder point as a function of pulse duration.

## 5. Characteristics

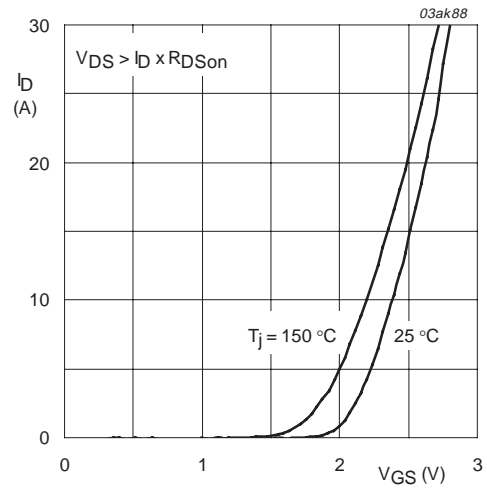
**Table 4: Characteristics**
 $T_j = 25\text{ °C}$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\ \mu\text{A}$ ; $V_{GS} = 0\ \text{V}$ $T_j = 25\text{ °C}$	30	-	-	V
		$T_j = -55\text{ °C}$	27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\ \text{mA}$ ; $V_{DS} = V_{GS}$ ; <b>Figure 9</b> $T_j = 25\text{ °C}$	1	1.5	2	V
		$T_j = 150\text{ °C}$	0.6	-	-	V
		$T_j = -55\text{ °C}$	-	-	2.2	V
$I_{DSS}$	drain-source leakage current	$V_{DS} = 30\ \text{V}$ ; $V_{GS} = 0\ \text{V}$ $T_j = 25\text{ °C}$	-	0.05	1	$\mu\text{A}$
		$T_j = 150\text{ °C}$	-	-	500	$\mu\text{A}$
$I_{GSS}$	gate-source leakage current	$V_{GS} = \pm 16\ \text{V}$ ; $V_{DS} = 0\ \text{V}$	-	10	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5\ \text{V}$ ; $I_D = 13\ \text{A}$ ; <b>Figure 7 and 8</b> $T_j = 25\text{ °C}$	-	6.6	7.7	m $\Omega$
		$T_j = 150\text{ °C}$	-	11.2	13.1	m $\Omega$
		$V_{GS} = 10\ \text{V}$ ; $I_D = 14\ \text{A}$ ; <b>Figure 7 and 8</b>	-	5.5	6.5	m $\Omega$
<b>Dynamic characteristics</b>						
$Q_{g(tot)}$	total gate charge	$I_D = 14\ \text{A}$ ; $V_{DD} = 15\ \text{V}$ ; $V_{GS} = 4.5\ \text{V}$ ; <b>Figure 13</b>	-	30.3	-	nC
$Q_{gs}$	gate-source charge		-	7.8	-	nC
$Q_{gd}$	gate-drain (Miller) charge		-	11.4	-	nC
$C_{iss}$	input capacitance	$V_{GS} = 0\ \text{V}$ ; $V_{DS} = 20\ \text{V}$ ; $f = 1\ \text{MHz}$ ; <b>Figure 11</b>	-	2800	-	pF
$C_{oss}$	output capacitance		-	670	-	pF
$C_{rss}$	reverse transfer capacitance		-	320	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DD} = 15\ \text{V}$ ; $R_L = 15\ \Omega$ ; $V_{GS} = 10\ \text{V}$ ; $R_G = 6\ \Omega$	-	11	-	ns
$t_r$	rise time		-	10	-	ns
$t_{d(off)}$	turn-off delay time		-	80	-	ns
$t_f$	fall time		-	40	-	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain (diode forward) voltage	$I_S = 2.3\ \text{A}$ ; $V_{GS} = 0\ \text{V}$ ; <b>Figure 12</b>	-	0.72	1.2	V



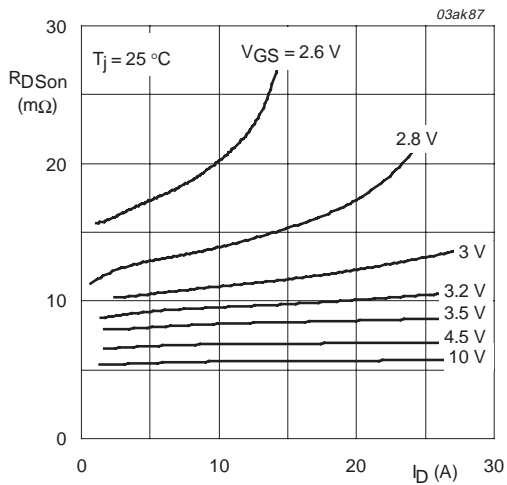
$T_j = 25\text{ }^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



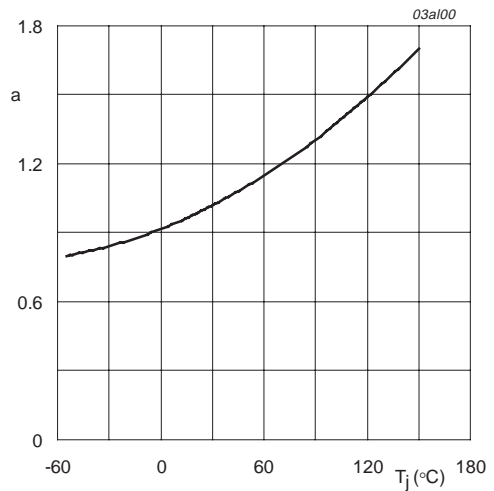
$T_j = 25\text{ }^\circ\text{C}$  and  $150\text{ }^\circ\text{C}$ ;  $V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



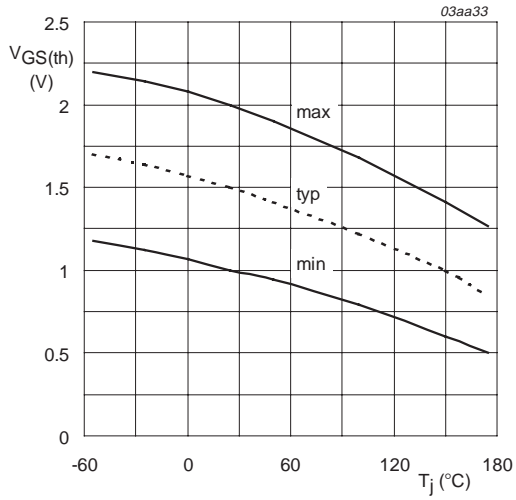
$T_j = 25\text{ }^\circ\text{C}$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



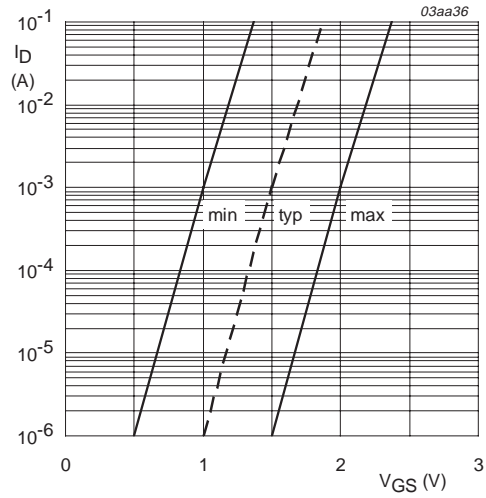
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



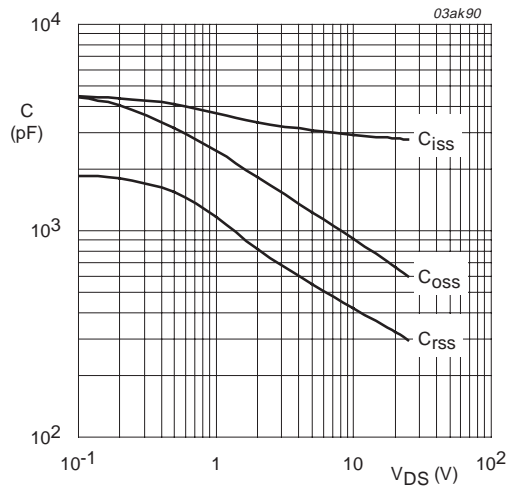
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



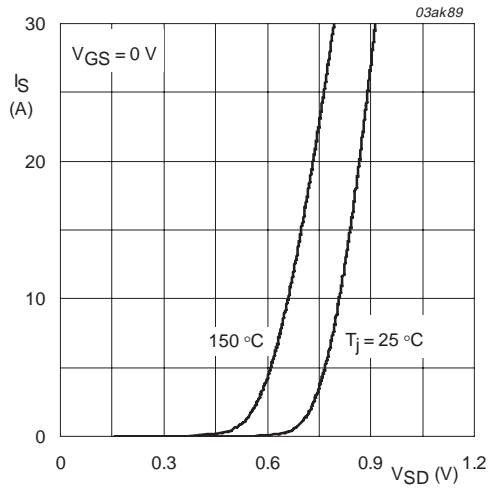
$T_j = 25 \text{ °C}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



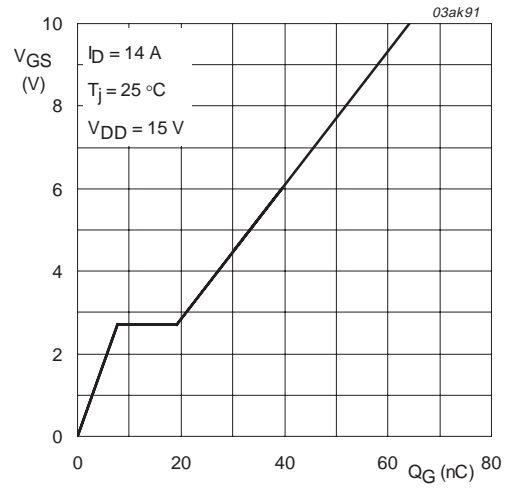
$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



$T_J = 25\text{ }^\circ\text{C}$  and  $150\text{ }^\circ\text{C}$ ;  $V_{GS} = 0\text{ V}$

**Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.**



$I_D = 14\text{ A}$ ;  $V_{DD} = 15\text{ V}$

**Fig 13. Gate-source voltage as a function of gate charge; typical values.**



6. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1

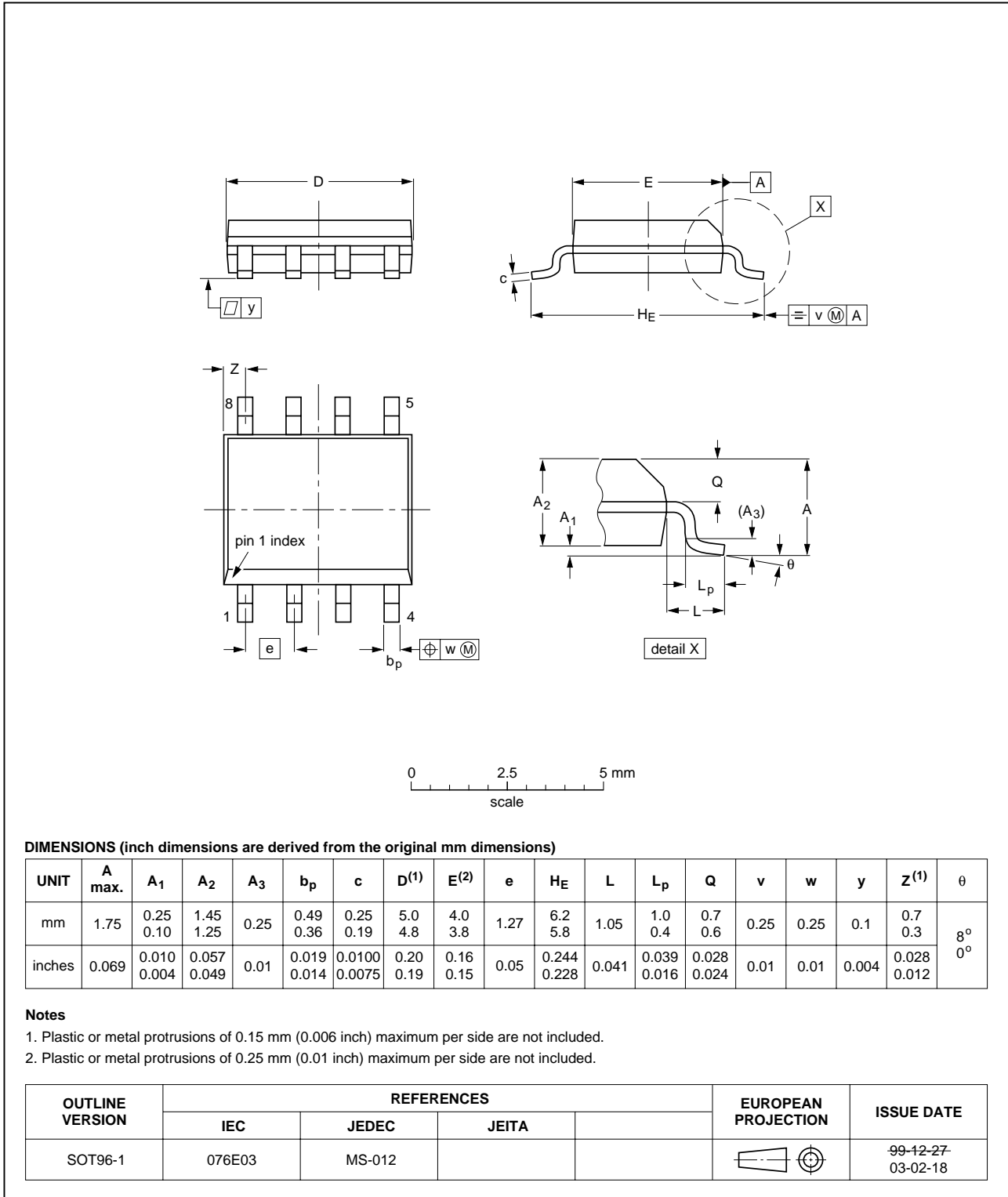


Fig 14. SOT96-1 (SO8).

## 7. Revision history

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Table 5: Revision history

Rev	Date	CPCN	Description
02	20030410	-	<b>Product data (9397 750 11367)</b> Modifications: <ul style="list-style-type: none"><li>• Typographical error corrected in typical values of <math>Q_{GS}</math>, <math>Q_{GD}</math> in <b>Section 5 “Characteristics”</b></li></ul>
01	20021212	-	<b>Product data (9397 750 10743)</b>

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